What is claimed is:

1. A prefetch-type FCRAM having an improved data write control circuit in a semiconductor memory device including a memory cell array, a plurality of address pins, and a plurality of data pins, the prefetch-type FCRAM comprising:

a command decoder which outputs control commands including first and second write commands in response to predetermined external input signals;

a row decoder which decodes a row address signal input by the address pins and activates a wordline of the memory cell array corresponding to the decoded row address signal;

a column decoder which decodes a column address signal input by the address pins and activates a column select line of the memory cell array corresponding to the decoded column address signal;

a data input buffer which receives input data from the plurality of data pins and outputs the input data in synchronization with a predetermined clock signal;

a data output buffer which outputs output data read from the memory cell array to the plurality of data pins; and

a valid write window buffer which outputs a data masking control signal that controls the masking of input data in response to a combined address signal input by the address pins,

wherein the column decoder disables a column select line where data to be masked among the input data will be input in response to the data masking control signal.

2. The prefetch-type FCRAM of claim 1, wherein the combined address signal is some of a plurality of bits applied to the address pins when the second write command is applied.

3. The prefetch-type FCRAM of claim 1, wherein the combined address signal comprises:

a first address signal used for controlling the prevention of the input data from being written; and

a second address signal used for controlling a sequence of writing the input data.

4. The prefetch-type FCRAM of claim 3, wherein the valid write window buffer comprises:

an input buffer and decoder which decodes the first address signal and outputs a predetermined write control signal;

a valid write window control circuit which outputs a write information signal indicating whether to mask each bit of the input data, every four bits of which are input in series through the plurality of data pins, in response to the write control signal; and

a sequence control circuit which determines a sequence of writing the input data in response to the second address signal and outputs the data masking control signal in response to the sequence and the write information signal.

5. The prefetch-type FCRAM of claim 4, wherein the valid write window control circuit comprises:

a write information generation circuit which outputs an internal write information signal in response to the write control signal; and

an output circuit which latches the internal write information signal and outputs the write information signal.

6. The prefetch-type FCRAM of claim 5, wherein the write information generation circuit comprises first through fourth write information generators which generate an internal write information signal in response to the write control signal, and the output circuit comprises first through fourth latches connected to the first through fourth write information generators, respectively, which latch the internal write information signal and output the write information signal.

7. The prefetch-type FCRAM of claim 6, wherein the first through fourth latches each include an initial value setting circuit for maintaining initial voltage levels of input ports of the first through fourth latches, respectively, at a predetermined level in response to a predetermined internal control signal when power is applied.

8. The prefetch-type FCRAM of claim 6, wherein each of the first through fourth write information generators comprises:

a NAND gate, which performs a logic operation on the write control signal;

a plurality of inverters which invert an output signal of the NAND gate and outputs the inverted signal; and

a plurality of transmission gates which are turned on in response to the output signals of the NAND gate and the plurality of inverters and then output the internal write information signal.

9. The prefetch-type FCRAM of claim 8, wherein the plurality of transmission gates of at least one of the first through fourth write information generators have input ports connected to ground.

10. The prefetch-type FCRAM of claim 8, wherein the plurality of transmission gates of some of the first through fourth write information generators have some input ports connected to ground and other input ports connected to a predetermined internal voltage.

11. The prefetch-type FCRAM of claim 8, wherein the plurality of transmission gates of at least one of the first through fourth write information generators have input ports connected to a predetermined internal voltage.

12. The prefetch-type FCRAM of claim 11, wherein the first through fourth latches each include an inverter for inverting and outputting its corresponding latch's output signal.

13. The prefetch-type FCRAM of claim 1, wherein the FCRAM is a 4-bit FCRAM.

14. A method of masking input data in a semiconductor memory device including a memory cell array, a plurality of address pins, and a plurality of data pins, the method comprising:

(a) generating control commands including first and second write commands in response to predetermined external input signals;

(b) receiving a row address signal, a column address signal, and an combined address signal through the plurality of address pins;

(c) receiving the input data through the plurality of data pins;

(d) decoding the row address signal and activating a wordline of the memory cell array corresponding to the decoded row address signal;

(e) decoding the column address signal and enabling a column select line of the memory cell array corresponding to the decoded column address signal;

(f) generating a data masking control signal that controls the masking of input data in response to the combined address signal; and

(g) disabling, using a column decoder, a column select line where data to be masked among the input data will be input in response to the data masking control signal.

15. The method of claim 14, wherein the combined address signal is some of a plurality of bits applied to the address pins when the second write command is applied.